Section 32. High-Level Device Integration

HIGHLIGHTS

This section of the manual contains the following topics:

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High-Level Device Integration

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32.1   INTRODUCTION

At their highest level of functionality, PIC24F devices incorporate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

* Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options, and change them if needed, during run time
* Device Identification – Permitting electronic confirmation of a device part number and revision level in the target application
* On-Chip Voltage Regulator – Permitting the device to be used over a range of application voltage levels

32.2   DEVICE CONFIGURATION

The basic behavior and operation of PIC24F devices are set by the device Configuration bits. These allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In PIC24F family devices, device Configuration bits are mapped into the device's program memory space, starting at location F80000h. This is beyond the user program memory space, and in fact, belongs to the configuration memory space (800000h-FFFFFFh). These Configuration bits are implemented as volatile memory, which means that configuration data must be loaded each time the device is powered up. The actual configuration data is stored in the two words at the top of the on-chip program memory space, known as the Flash Configuration Words. These are packed representations of the actual device Configuration bits, whose actual locations are distributed among several locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during all types of device Resets.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once. After a bit is initially written during a power cycle or any Reset, it cannot be written to again. Any change of a Configuration bit (but not a change to a Flash Configuration Word) causes a Configuration Mismatch (CM) Reset.

A list of the available Configuration bit options is shown in Table 32-1. A more complete description of each Configuration bit and its operation is described in the relevant section of the *"PIC24F Family Reference Manual"*. Note that not all bits described here are available on all devices.

For specific information on the location of device Configuration Words and Configuration bit mapping for a particular device, refer to the specific device data sheet.

32.2.1   Considerations When Using Flash Configuration Words

When creating applications for PIC24F devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

The upper byte of both Flash Configuration Words in program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

As previously mentioned, changes to the actual device Configuration bits during run time will cause a Configuration Mismatch Reset. This does not prevent changes to Flash Configuration Words during normal operation. This also makes it possible for an application to change its own hardware configuration by writing new data to one or both Flash Configuration Words, then executing a RESET command.

Table 32-1:   PIC24F Device Configuration Bits

Configuration Bit	Function
COE	Enables clip-on emulation with external devices; device is held in Reset.
DEBUG	Enables background debugger operation with external device control.
FCKSM	Configures device clock switching and Fail-Safe Clock Monitor (2 bits, 3 configuration options).
FNOSC	Selects initial (default) device oscillator (3 bits, up to 8 configuration options).
FWDTEN	Enables Watchdog Timer.
FWPSA	Selects WDT prescaler.
GCP	Enables code protection for the program memory space.
GWRP	Enables write/erase protection for program memory.
I2CxSEL	Selects standard or alternate I/O pin mapping of SCLx and SDAx.
ICS	Selects which ICSP™ port is used with ICD (2 bits, up to 4 options).
IESO	Enables Two-Speed Start-up.
IOL1WAY	Selects one-time or unrestricted run-time changes to peripheral mapping.
JTAGEN	Enables dedicated JTAG port and disables corresponding I/O ports on designated pins.
OSCIOFCN	Selects function of OSC2 pin (I/O port or CLKO) in certain external oscillator modes.
POSCMD	Selects primary (external) oscillator configuration (2 bits, 4 configurations).
WDTPS	Selects WDT postscaler (4 bits, up to 16 configuration options).
WINDIS	Selects Windowed Operation mode for Watchdog Timer.

32.3   DEVICE IDENTIFICATION

PIC24F devices have two registers that provide device-specific identification information. These read-only registers are located near the end of the device configuration space, starting at FF0000h. Like the Flash Configuration Words, the device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using table read instructions.

The DEVID register at FF0000h (Register 32-1) identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register at FF0002h (Register 32-2) identifies the particular silicon revision for that device in terms of major and minor revision levels ("letter and dot revision" format).

For any given family of PIC24F devices, the corresponding device data sheet provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a silicon revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in part-specific literature, such as device silicon errata, or through Microchip's development tools, such as MPLAB® IDE. For assistance with interpreting values of DEVREV, please contact Microchip technical support or your local Microchip representative.

Register 32-1:   DEVID: Device ID Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U	U	R	R	R	R	R	R
—	—	FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2
bit 15							bit 8

R	R	R	R	R	R	R	R
FAMID1	FAMID0	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as '0'

bit 23-14   **Unimplemented:** Read as '0'

bit 13-6   **FAMID7:FAMID0:** Device Family Identifier bits

bit 5-0   **DEV5:DEV0:** Individual Device Identifier bits

Register 32-2:   DEVREV: Device Revision Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	U	U	U	R
r	r	r	r	—	—	—	MAJRV2
bit 15							bit 8

R	R	U	U	U	R	R	R
MAJRV1	MAJRV0	—	—	—	DOT2	DOT1	DOT0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as '0'

bit 23-16   **Unimplemented:** Read as '0'

bit 15-12   **Reserved:** For factory use only

bit 11-9   **Unimplemented:** Read as '0'

bit 8-6   **MAJRV2:MAJRV0:** Major Revision Identifier bits

bit 5-3   **Unimplemented:** Read as '0'

bit 2-0   **DOT2:DOT0:** Minor Revision Identifier bits

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32.4 ON-CHIP VOLTAGE REGULATION

The PIC24 family powers its core digital logic at a nominal 2.5V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all PIC24 family devices incorporate an on-chip regulator that allows the device to run its core logic from V$_{DD}$.

PIC24F family devices use two different on-chip regulators: those that are positively enabled by applying a control signal and those that are positively disabled with a control signal. In the former, the regulator is enabled by supplying it with V$_{DD}$, while in the latter, the regulator is disabled when supplied with V$_{DD}$. For devices with positive enable regulators, the regulator control pin is named ENVREG. For devices with positive disable regulators, the control pin is named DISVREG.

When enabled, the regulator draws power from the V$_{DD}$ pins to provide power to the digital logic. When disabled, power for the core logic must be supplied to the device on the V$_{DDCORE}$/V$_{CAP}$ pin. This can be done by supplying separate V$_{DD}$ and V$_{DDCORE}$ voltages to allow the I/O pins to run at higher voltage levels (nominal 2.5V and 3.3V for V$_{DDCORE}$ and V$_{DD}$, respectively). If the higher voltage is not required, the V$_{DDCORE}$/V$_{CAP}$ and V$_{DD}$ pins can be tied together to operate at a lower nominal voltage. Refer to the device data sheet for device-specific voltage limitations.

A capacitor with a low effective series resistance (made of tantalum or ceramic) must be connected to the V$_{DDCORE}$/V$_{CAP}$ pin. The recommended ESR (Equivalent Series Resistance) is 3 ohms maximum. This helps maintain the stability of the regulator. The recommended value for the filter capacitor is provided in the Electrical Characteristics section of the specific device data sheet.

Possible configurations for both positive enable and positive disable regulators are shown in Figure 32-1.

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Figure 32-1:   Connections for the On-Chip Regulator (Positive Enable and Positive Disable)

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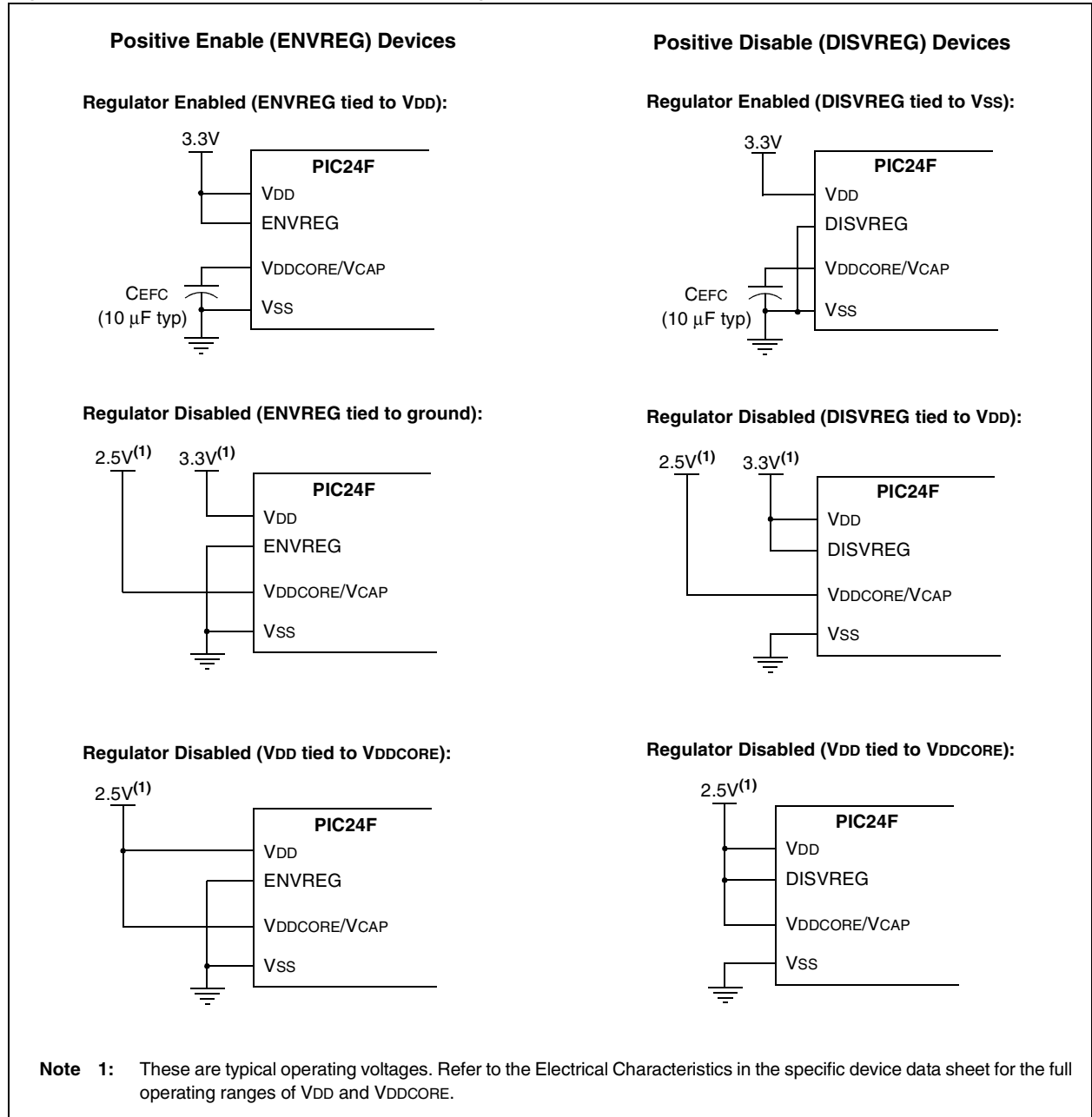
32.4.1   On-Chip Regulator and Power-on Reset (POR)

When the voltage regulator is enabled, it takes approximately 20 μs for it to generate output. During this time, designated as T$_{STARTUP}$, code execution is disabled. T$_{STARTUP}$ is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of 64 ms nominal delay at device start-up.

32.4.2   On-Chip Regulator and Brown-out Reset (BOR)

When the on-chip regulator is enabled, the PIC24 family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain device operation, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are listed in the specific device data sheet.

32.4.3   Voltage Regulator Tracking Mode

When it is enabled, the on-chip regulator provides a constant voltage of 2.5V nominal to the digital core logic. The regulator can provide this level from a V$_{DD}$ of about 2.7V, all the way up to the device's V$_{DDMAX}$. It does not have the capability to boost V$_{DD}$ levels below 2.5V. In order to prevent "brown out" conditions when the voltage drops too low for the regulator, devices with the Low-Voltage Detect (LVD) feature enter a Tracking mode. In Tracking mode, the regulator output follows V$_{DD}$, with a typical voltage drop of 100 mV.

When the device enters Tracking mode, it is no longer possible to operate at full speed. To provide information about when the device enters Tracking mode, the on-chip regulator includes a simple, Low-Voltage Detect circuit. When V$_{DD}$ drops below full-speed operating voltage, the circuit sets the Low-Voltage Detect Interrupt Flag, LVDIF. This can be used to generate an interrupt and put the application into a low-power operational mode or trigger an orderly shut-down. Low-Voltage Detection is only available when the regulator is enabled. If V$_{DD}$ drops below minimum Tracking mode voltage, a Brown-out Reset will be generated.

32.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Level Device Integration are:

Title   **Application Note #**

No related application notes at this time.

> **Note:**   Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

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32.6 REVISION HISTORY

Revision A (January 2007)

This is the initial released revision of this document.

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NOTES: